controls the memory device shown in FIG. 3. Address represents row and column address signals from the microcomputer. WL0 and WL1 represent the respective high and low voltages of the word lines WL0 and WL1, respectively. SA0-0, SA0-1, ..., and SA0-n represent the respective voltages of the sense amplifiers 30A-0, 30A-1, ..., and 30A-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively. SA1-0, SA1-1, ..., and SA1-n represent the respective voltages of the sense amplifiers 30B-0, 30B-1, ..., and 30B-n on the pairs of bit lines BL0 and BLB0, BL1 and BLB1, ..., and BLn and BLBn, respectively.

Data Out represents output data outputted to the read data bus through the read gates. Data In represents input data supplied from the write data bus to the write gates. TGSel represents a gate select signal indicative of either the transfer gate 20A or 20B, from the microcomputer. TG0 and TG1 represent the control signals supplied to the transfer gates 20A and 20B, respectively.

The command Command first indicates ACT to a row address RA0 so as to activate the row address RA0, thus the word line WL0 first changes from low level to high level, and thus the command Command changes to Read so as to read column addresses CA00 and CA01. After that, the gate select signal TGSel changes to TG0 so as to change the gate signal TG0 from low level to high level, and thus the transfer gate 20A is turned on so as to allow the sense amplifiers 30A-0 and 30A-1 to amplify and latch "1" data of the memory cells 10-0 and 10-1, respectively. Then, the sense amplifiers 30A-0 and 30A-1 output the amplified data